Claims

What is claimed is:

1. A method for recovering an original bit stream from a received chip stream in a communication system, comprising the steps of:

maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and

synchronizing a bit clock by using the history of correlation.

2. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming a correlator output over all possible sample positions for the bit clock.

3. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming a correlator output over a finite window of sample positions for the bit clock.

4. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

5. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

6. The method of claim 1, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

7. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

8. The method of claim 6, wherein the step of synchronizing the bit clock is based on the histogram of the counters that exceed a preset threshold.

9. The method of claim 7, wherein the step of synchronizing the bit clock is based on the histogram of the accumulators that exceed a preset threshold.

10. The method of claim 1, wherein the step of synchronizing the bit clock is based on a calculated average sample position for the bit clock.

11. The method of claim 2, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

12. The method of claim 2, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

13. The method of claim 3, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

14. The method of claim 3, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

15. The method of claim 6, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

16. The method of claim 6, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

17. The method of claim 7, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

18. The method of claim 7, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

19. The method of claim 8, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

20. The method of claim 8, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

21. The method of claim 9, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

22. The method of claim 9, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

23. The method of claim 10, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

24. The method of claim 10, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

25. The method of claim 2, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

26. The method of claim 2, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

27. The method of claim 3, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

28. The method of claim 3, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

29. The method of claim 8, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

30. The method of claim 8, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

31. The method of claim 9, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

32. The method of claim 9, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

33. The method of claim 10, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator

output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

34. The method of claim 10, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

35. The method of claim 2, wherein the step of synchronizing the bit clock is based on the histogram of a plurality of counters that exceed a preset threshold.

36. The method of claim 2, wherein the step of synchronizing the bit clock is based on the histogram of a plurality of accumulators that exceed a preset threshold.

37. The method of claim 2, wherein the step of synchronizing the bit clock is based on a calculated average sample position for the bit clock.

38. The method of claim 3, wherein the step of synchronizing the bit clock is based on the histogram of a plurality of counters that exceed a preset threshold.

39. The method of claim 3, wherein the step of synchronizing the bit clock is based on the histogram of a plurality of accumulators that exceed a preset threshold.

40. The method of claim 3, wherein the step of synchronizing the bit clock is based on a calculated average sample position for the bit clock.

41. A pseudo-noise encoded digital data clock recovery circuit for recovering an original bit stream from a received chip stream, comprising:

a correlator for correlating a pseudo-noise sequence with the received chip stream and generating a correlator output, the pseudo-noise sequence modulating the original bit stream;

a phase controller, coupled to the correlator, being configured and arranged to histogram the correlator output of the correlator over the plurality of bit periods; and

a bit clock generator, coupled to the phase controller, for generating a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream, the bit clock generator using the histogram of the correlator output to select/adjust the sample position for the bit clock.

42. The circuit of claim 41, wherein the phase controller includes a plurality of counters to histogram the correlator output over all sample positions in a bit period for the plurality of consecutive bit periods, each of the counters corresponding to each of the sample positions within the bit period.

43. The circuit of claim 42, wherein each of the counters is incremented when a

corresponding thresholded correlator output generates a spike at the corresponding sample position.

44. The circuit of claim 43, wherein the bit clock generator adjusts the sample position of the bit clock to a position where the corresponding counter exceeds a threshold.

45. The circuit of claim 44, wherein the bit clock generator retains the same sample position of the bit clock where no counters exceed the threshold.

46. The circuit of claim 41, wherein the phase controller includes a plurality of counters to histogram the correlator output over a finite window of sample positions for the bit clock.

47. The circuit of claim 41, wherein the phase controller histograms the correlator output for a finite number of bit periods and restarts histogramming after the finite number of bit periods.

48. The circuit of claim 41, wherein the phase controller histograms continuously by digitally low pass filtering the correlator output.

49. The circuit of claim 41, further comprising a comparator which compares the correlator output to a threshold and generates a thresholded correlator output, wherein the phase controller histograms the thresholded correlator output with a plurality of counters.

50. The circuit of claim 41, wherein the phase controller includes a plurality of accumulators to histogram the correlator output directly.

51. The circuit of claim 49, wherein the bit clock is based on the histogram of the counters that exceed a preset threshold.

52. The circuit of claim 50, wherein the bit clock is based on the histogram of the accumulators that exceed a preset threshold.

53. The circuit of claim 41, wherein the bit clock is based on a calculated average sample position for the bit clock.

54. A communication system, comprising:

a transmitter, the transmitter modulating an original bit stream into a transmitted chip stream by a pseudo-noise sequence, the transmitted chip stream being transmitted to a receiver via a transmission media;

the transmission media;

the receiver receiving a received chip stream; and

a clock recovery circuit being coupled to the receiver, the clock recovery circuit recovering the original bit stream from the received chip stream, comprising:

a correlator for correlating a pseudo-noise sequence with the received chip stream and generating a correlator output, the pseudo-noise sequence modulating the original bit stream;

a phase controller, coupled to the correlator, being configured and arranged to histogram the correlator output of the correlator over the plurality of bit periods; and

a bit clock generator, coupled to the phase controller, for generating a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream, the bit clock generator using the histogram of the correlator output to select/adjust the sample position for the bit clock.

55. A computer program storage medium readable by a computing system and encoding a computer program of instructions for executing a computer process for recovering an original bit stream from a received chip stream, the computer process comprising:

maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and

synchronizing a bit clock by using the history of correlation.

56. A computer data signal embodied in a carrier wave readable by a computing system and encoding a computer program of instructions for executing a computer process for recovering an original bit stream from a received chip stream, the computer process comprising:

maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and

synchronizing a bit clock by using the history of correlation.